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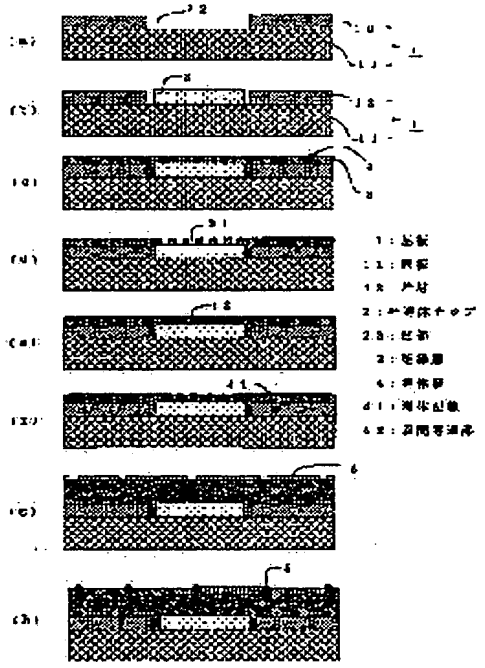
(71)Applicant : MITSUBISHI ELECTRIC CORP
(72)Inventor : YANAGIURA SATOSHI
OKA SEIJI
FUJIOKA HIROFUMI

(54) SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor device for enabling high density wiring and preventing peeling at the time of reflow.
SOLUTION: A substrate 1 is composed of a bottom plate 11 composed of a metal and a frame material 12 composed of a resin composite material and is provided with a recessed part 22. A semiconductor chip 2 is buried in the recessed part 22, an insulation layer 3 provided with an inter-layer conductive part 42 on the terminal of the semiconductor chip 2 is provided on it and the insulation layer 3 is provided with conductor wiring 41 in continuity with the inter-layer conductive part. Further, the insulation layer provided with a stud via and a conductor wiring pattern are laminated on the conductor wiring 41 by a build-up method.



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[Claim(s)]

[Claim 1] The substrate which has a crevice, the semiconductor chip embedded in the above-mentioned crevice, the above-mentioned semiconductor chip, and a substrate front face are covered. The insulating layer which has opening in the connection terminal area of the above-mentioned semiconductor chip, the layer flow section which gave the flow for the above-mentioned opening with the conductive ingredient, the conductor which prepares in a list at the above-mentioned insulating layer, and flows with the above-mentioned layer flow section -- with the resin composite material with which it is the semiconductor device equipped with wiring, and the above-mentioned substrate formed the thermal buyer, or the bottom plate which consists of a metal The semiconductor device characterized by having the frame material which pastes this bottom plate, has a larger through tube than the above-mentioned semiconductor chip, and consists of polyimide or resin composite material.

[Claim 2] a conductor -- the insulating layer which has on wiring stud beer which filled up the inside of beer with the conductive ingredient by the build up method, and a conductor -- the semiconductor device according to claim 1 characterized by carrying out the laminating of the wiring one by one.

[Claim 3] The semiconductor device according to claim 1 or 2 characterized by resin composite material consisting of resin, and glass fabrics, a nonwoven glass fabric, a polyamide system nonwoven fabric or a liquid crystal polymer system nonwoven fabric.

[Detailed Description of the Invention]

[0001]

[Field of the Invention] Especially this invention relates to the semiconductor device which mounted electronic parts, such as a semiconductor chip.

[0002]

[Description of the Prior Art] Although the chip of a package and the connection of an INTAPOZA substrate containing a semi-conductor INTAPOZA substrate are conventionally made by wire bond or bump connection, a limitation is in detailed-ization of alignment precision or an electrode, and it is thought that it is difficult to deal with the pitch of 0.4mm or less.

[0003] As this cure, a high density wiring semiconductor chip is embedded by face up at a substrate, and the approach of pulling out an outer bump is indicated by the following patent official report. Namely, an external connection terminal embeds the chip prepared in the front face in a base material crevice at JP,4-25038,A. After preparing an insulating layer besides and forming a beer hall in a part for the above-mentioned external connection terminal area, it is what formed the upper circuit and the bump and formed the solder resist in the other field. As the above-mentioned base material What prepared the crevice by etching or mechanical cutting, and the thing which prepared the crevice with mechanical cutting or injection molding using thermosetting resin etc. are indicated using metals, such as aluminum.

[0004] Moreover, a semiconductor chip as well as the above-mentioned official report is embedded at JP,9-321408,A, it is what was further multilayered with the build up, and what was formed beginning to delete the above-mentioned crevice, and the pierced thing are indicated, using a stud bump as an external connection terminal of a semiconductor chip.

[0005] Moreover, using the substrate which stuck two substrates in which the through tube of the magnitude of a semiconductor chip was formed in the same part on both sides of one substrate, by embedding a semiconductor chip at the above-mentioned through tube, high density assembly is performed and the thing using copper-clad laminates, such as glass epoxy, as the above-mentioned substrate is indicated by JP,1-175297,A.

[0006]
[Problem(s) to be Solved by the Invention] However, although what sufficient leading about could not do but formed the crevice in the metal base front face as a cure against heat dissipation was used for the thing given in JP,4-25038,A since expansion of wiring was one layer, it had the technical problem that high cost started processing or exfoliation arose between a metal base and an insulating layer according to the difference of the thermal expansion of a metal base and the insulating layer prepared on this at the time of a reflow. Moreover, although the base material which consists of resin machined resin, or injection molding of the thermoplastics was carried out and it had been obtained, high cost required the former, and bad [adhesion with the insulating layer coated from a top since the release agent is contained], since the coefficient of thermal expansion of the latter of the base material itself was large, it had the technical problem that a coefficient-of-thermal-expansion difference with a semiconductor chip is large, and a semiconductor chip broke at the time of a reflow, or it was easy to produce exfoliation between semiconductor chips. Furthermore, by the latter, the heat dissipation nature of a chip is bad and causes [of a chip] malfunction.
[0007] Since a stud bump was used for a thing given in JP,9-321408,A and it was difficult to acquire stud beer structure, it was unsuitable for wiring leading about of high density, and since the ingredient of the substrate which began to delete a crevice was not taken into consideration, the technical problem which exfoliation tends to produce that heat dissipation of a chip was inadequate occurred between semiconductor chips like the above at the time of a reflow.
[0008] Thermal conductivity is bad and the thing given in JP,1-175297,A had a technical problem in heat dissipation nature, although copper-clad laminates, such as glass epoxy, were used as the 1st and 2nd substrate (equivalent to a bottom plate and frame material).
[0009] This invention is obtained in the semiconductor device which was made in order to cancel this technical problem, and is excellent in heat dissipation nature and by which generating of the exfoliation at the time of a reflow was prevented.
[0010]
[Means for Solving the Problem] The substrate with which the 1st semiconductor device concerning this invention has a crevice, the semiconductor chip embedded in the above-mentioned crevice, The insulating layer which covers the above-mentioned semiconductor chip and a substrate front face, and has opening in the connection terminal area of the above-mentioned semiconductor chip, The above-mentioned opening is prepared in the layer flow section and the list which took the flow with the conductive ingredient at the above-mentioned insulating layer. the above-mentioned layer flow section and the flowing conductor -- with the resin composite material with which it is the semiconductor device equipped with wiring, and the above-mentioned substrate formed the thermal buyer, or the bottom plate which consists of a metal This bottom plate is pasted, and it has a larger through tube than the above-mentioned semiconductor chip, and has the frame material which consists of polyimide or resin composite material.
[0011] the 2nd semiconductor device concerning this invention -- the 1st semiconductor device of the above -- setting -- a conductor -- the insulating layer which has on wiring stud beer which filled up the inside of beer with the conductive ingredient by the build up method, and a conductor -- the laminating of the wiring is carried out one by one.
[0012] In the 1st or 2nd semiconductor device of the above, as for the 3rd semiconductor device concerning this invention, resin composite material consists of resin, and glass fabrics, a nonwoven glass fabric, a polyamide system nonwoven fabric or a liquid crystal polymer system nonwoven fabric.

[0013]

[Embodiment of the Invention] the explanatory view showing the process at which gestalt 1. drawing 1 [of operation] (a) - (h) manufactures the semiconductor device of the gestalt of operation of this invention -- it is -- the inside of drawing, and 1 -- a substrate -- it is -- from a bottom plate 11 and the frame material 12 -- becoming -- 2 -- a semiconductor chip and 22 -- a crevice and 3 -- an insulating layer and 31 -- opening and 4 -- a conductor layer and 41 -- a conductor -- as for the layer flow section and 5, wiring and 42 are [a bump and 6] solder resists.

[0014] The substrate 1 which has a crevice concerning the gestalt of operation of this invention consists of a bottom plate 11 and frame material 12, a crevice 22 is formed in a substrate 1 by the frame material 12, and the frame material 12 has a larger through tube than the semiconductor chip 2 which carries out face up of the semiconductor chip 2 to a bottom plate 11, and can lay it.

[0015] As a bottom plate 11, metals, such as copper, 42 alloys, or aluminum, or resin composite material in which the thermal buyer was formed is used, and it is effective in excelling in heat dissipation nature. As a resinous principle of resin composite material, epoxy, poly para-phenylene system resin, or BT resin is used, and a liquid crystal polymer nonwoven fabric, a polyamide fiber nonwoven fabric, glass fabrics, or a nonwoven glass fabric is used as a reinforcement component. the thing of the through hole formed in order to miss the heat generated in the bottom plate upper part (chip mounting side) with the thermal buyer on a bottom plate background -- it is -- a bottom plate -- the through tube of 0.6mm of phi0.25 mm-phi -- a drill etc. -- opening -- the porous wall or a hole -- the whole is filled up with metal plating or a high temperature conduction ingredient. A high temperature conduction ingredient is what filled up organic resin with metal particles or a ceramic particle, and thermal conductivity is the thing of 1.0 or more W/mK. When a thermal buyer is prepared in a bottom plate using the resin composite material which stuck copper foil on the side used as the rear face, the heat which was transmitted in the thermal buyer and turned to the background gets across to the copper foil on a bottom plate background further, and radiates heat efficiently in air from there, and heat dissipation nature is further strengthened by preparing a radiation fin, a fan, etc. on copper foil. Moreover, when using for a bottom plate the resin composite material which stuck copper foil on the both sides, adhesion with frame material can be improved by removing the metal layer of the location in which a thermal buyer is formed in the location in which a semiconductor chip is prepared, and heat dissipation nature is maintained, and frame material is prepared. Moreover, when a metal is used as a bottom plate 11, while excelling in heat dissipation nature, since the coefficient-of-thermal-expansion difference with a semiconductor chip 2 is small, the exfoliation at the time of a reflow can be prevented.

[0016] Moreover, as frame material 12, coefficient of thermal expansion of a polyimide film is small, and although others, a polyimide film, or a liquid crystal polymer film is used, since adhesion with an insulating layer is good, it can prevent the exfoliation at the time of a reflow, while excelling in thermal resistance. [prepreg / above-mentioned / resin composite-material]

[0017] furthermore, the semiconductor package concerning this invention -- one side of a bottom plate -- an insulating layer and a conductor -- since wiring is stacked and it dies, a rigid high bottom plate which curvature does not generate in a back process, and a frame board are desirable to some extent, for example, when using copper for a bottom plate, the copper plate more than 0.5mm thickness is desirable, and the thickness of a frame board has good thickness and this extent of the semiconductor chip to be used.

[0018] moreover, the build up method -- an insulating layer and a conductor -- when

carrying out the laminating of the wiring and giving a multilayer interconnection, by using the above-mentioned substrate concerning the gestalt of this operation, heat can be efficiently radiated outside in the heat generated from a chip, and the temperature rise of a chip is pressed down and the effectiveness of preventing malfunction and destruction of a chip is acquired.

[0019] Next, the process which manufactures the semiconductor device of the gestalt of operation of this invention is explained using drawing 1 . First, the substrate 1 which has a crevice 22 is obtained by sticking the above-mentioned frame material 12 and a bottom plate 11 { drawing 1 (a)}. A heat press or the heat laminator of lamination is desirable in respect of mass-production nature. Although lamination is possible as it is when frame material is composite prepreg, in the case of a resin film, it is necessary to use adhesives.

[0020] Next, face up of the semiconductor chip is carried out to the crevice 22 of the substrate 1 obtained as mentioned above, and it is stuck on it { drawing 1 (b)}. It is desirable to use a thermally conductive high die bond agent for attachment from a viewpoint of high heat dissipation nature. Thermally conductive high die bond material is what was high-filled up with fillers, such as copper, silver, an alumina, a diamond, silicon nitride, or boron nitride, into an epoxy resin or polyimide resin, and 2.0 or more W/m-K is desirable as thermal conductivity.

[0021] Next, the insulating layer 3 of an eye is further formed from a top (drawing 1 (c)}.). Although any of liquefied resin and film resin and RCC (Resin Coated Copper) are sufficient as an insulating layer 3, the upper surface smoothness is important from a viewpoint which carries out a laminating to a multilayer, when the point is taken into consideration, a film or RCC is desirable, drawing shows the case where RCC is used as an insulating layer, and the conductor layer 4 is stuck on the insulating layer. When an insulating layer is RCC, in the case of a film, a laminating uses a vacuum laminator using a heat press or a vacuum laminator.

[0022] { Drawing 1 (d)} which forms opening 31 (Bahia hall) in an insulating layer 3 is able to form the Bahia hall by package by exposure and development, when the insulating layer has photosensitivity, and when it does not have photosensitivity, the Bahia hall is formed using laser light. As a laser light, the higher harmonic of carbon dioxide laser, an excimer laser, and an YAG laser is desirable. The area one-shot exposure which used the mask is possible for an excimer laser, and other laser serves as a beam exposure of every one hole. Moreover, when insulator layer residue does not remain in the Bahia hall pars basilaris ossis occipitalis when the Bahia hall is formed by laser, and copper foil is not attached to an insulator layer, in order to make coppering adhesion give an insulator layer, it is necessary to give any of permanganic acid down stream processing, a plasma treatment process, or an ozone water treatment process they are after the patterning process of an insulator layer.

[0023] The obtained Bahia hall 31 is filled up with a conductive ingredient, and the layer flow section 42 is formed in it { drawing 1 (e)}. Since the layer flow section 42 is formed by filling up opening 31 with a conductive ingredient, stud beer formation is attained and the high density assembly of it becomes possible. There are an approach using coppering as an approach with which it is filled up, and an approach using a conductive paste. When RCC is used for an insulating layer, the wiring formation by plating loess is attained by filling up the Bahia hall with a conductive paste. Even when using the screen-stencil which can be printed under reduced pressure when filling up the Bahia hall with a conductive paste cannot be desirable however print under reduced pressure on account of a facility, restoration of void loess is possible by hardening under pressurization. When copper foil is not attached to an insulating layer, it is desirable at the point that the approach filled up with

the Bahia hall by plating can shorten a process. Although it is necessary to use the special electrolytic plating liquid for beer philharmonic coppering plating after the usual electroless deposition to perform the Bahia hall restoration by coppering, these are marketed and are easily available. However, since thick Cu plating may be formed also in an insulator layer front face when beer is filled up with beer philharmonic coppering, it is necessary to make surface coppering thickness thin by half etching or polish if needed in that case.

[0024] next, the obtained conductor layer 4 -- the usual subtrust method -- a conductor -- { drawing 1 (f)} which forms wiring 41. Moreover, when performing detailed wiring formation, a semi ADETIBU coppering method may be applied. After this approach forms a plating resist pattern after electroless deposition formation, accumulates electrolytic plating on opening and performs wiring formation, it is for obtaining a detailed and thick copper circuit pattern by removing the electroless deposition which exfoliated the resist and remained between patterns by software etching.

[0025] further -- the insulating stratification, the Bahia hall formation, and the Bahia hall -- a conductor -- by repeating connection (or restoration) and wiring formation, multilayering of a build up wiring layer is attained, the semiconductor device of the gestalt of operation of this invention can be obtained, a solder resist 6 is further formed on an outermost layer pattern, and { drawing 1 (g)}, and the bump 5 and ball for connection are formed (drawing 1 (h)}.)

[0026]

[Example] A 405mmx340mm copper plate with an example 1. thickness of 0.5mm is used as a bottom plate 11, and silane coupling agent processing is carried out after oxide-film removal processing. Next, the substrate 1 which formed the crevice 22 is obtained by making into the frame material 12 what opened 28 holes (vertical 4 train, width 7 train) of 15mm angle in trade name:epoxy multi R-1766 and 250-micrometer thickness FR-5 {glass fabrics by Matsushita Electric Works, Ltd.} epoxy prepreg, and carrying out the press laminating of this to the above-mentioned copper plate.

[0027] After sticking a high temperature conductivity pressure sensitive adhesive sheet {trade name:T-gon2000 and the product made from the Sir magon INC} on the above-mentioned crevice 22, the semiconductor chip 2 of 14mm angle {staggered arrangement (2025 pin(s), diameter phiof putt (copper by which surface preparation was carried out)100micrometer, and shortest pitch 370micrometer)} is stuck by pressure by face up. Next, the photosensitive dry film (it abbreviates to DF) {trade name:ViaLux and the product made from Dupont} of 68-micrometer thickness is laminated from a top with a vacuum laminator, patterning is performed using ultraviolet rays according to a part for the terminal area of a chip, and phi75-micrometer beer hall hole is formed. Next, after performing a permanganic acid process (swelling, permanganic acid processing, and reduction) and performing surface roughening of DF, a conductor layer is formed on DF at the same time it performs electroless deposition and beer philharmonic electrolytic copper plating {the product made from a trade name:cube light and Ebara You G Light} and embeds a beer hole. At this time, conductor-layer thickness was 25 micrometers. Next, after carrying out half etching of the conductor layer and setting conductor-layer thickness to 10 micrometers, the etching dry film performed patterning of a conductor layer. The diameter of a land on beer set phi100micrometer and wiring last shipment to 30 micrometers / 30 micrometers.

[0028] Surface preparation (CZ processing) {trade name:dirty bond and the MEC COMPANY LTD. make} of the wiring on the obtained substrate is carried out, the Bahia hall beer-philharmonic-plated like the last process after a lamination in the photosensitive dry film {trade name:ViaLux and the product made from Dupont} of 50-micrometer

thickness and a conductor layer with a thickness of 10 micrometers are produced, and a circuit pattern is formed by etching. It accumulates one by one so that a conductor layer may turn into a total of nine layers at the same process as the following, and the solder resist which carried out opening of the terminal area to the maximum upper layer is formed. 28 semiconductor packages per substrate were obtained by finally cutting into the piece of an individual. It was 0.1-degree-C/W when the thermal resistance between the chip and bottom plate rear face of the obtained package was measured.

[0029] 405mmx340mm 42 alloy plate with an example 2. thickness of 0.5mm was used as the bottom plate 11, and silane coupling agent processing of this was carried out. Then, 250-micrometer thickness liquid crystal polymer nonwoven fabric and epoxy prepreg which opened 28 holes (vertical 4 train, width 7 train) of 15mm angle were made into the frame material 12, the press laminating of this was carried out to the above-mentioned alloy plate, and the substrate 1 which formed the crevice 22 was obtained. a crevice 22 -- a high temperature conductivity pressure sensitive adhesive sheet -- {-- trade name: -- after sticking T-gon2000 and} made from the Sir magon INC, the semiconductor chip 2 of 14mm angle {staggered arrangement (2025 pin(s), diameter phiof putt (copper [finishing / surface preparation])100micrometer, and shortest pitch 370micrometer)} is stuck by pressure by face up.

[0030] Next, the laminating of the RCC (resin thickness of 100 micrometers, 12 micrometers of copper foil thickness) {trade name:R-0870 and the Matsushita Electric Works, Ltd. make} was carried out from the top with a heat press, patterning was performed using carbon dioxide laser according to a part for the terminal area of a chip, and phi75-micrometer beer hall hole was formed. However, in order to remove the resin residue which remained in the beer bottom after this, hole cleaning was performed with the oxygen plasma. Next, the conductive paste {trade name which contained the silver coat copper filler in the epoxy resin: Polish removed the part which embedded} made from Kyoto EREKKUSU in the beer hole using the vacuum screen printer, and was protruded after heat-hardening.

[0031] Next, the etching dry film performed patterning of a conductor layer. The diameter of a land on beer set last shipment of phi100micrometer and wiring to 30 micrometers / 30 micrometers. wiring on the obtained substrate -- melanism -- it processes and the Bahia hall and circuit pattern with which laser punching and a conductive paste were filled up with RCC of 50-micrometer thickness like the last process behind the laminating are formed by etching. It accumulates one by one so that a conductor layer may turn into a total of nine layers at the same process as the following, and the solder resist which carried out opening of the terminal area to the maximum upper layer is formed. 28 semiconductor packages per substrate were obtained by finally cutting into the piece of an individual. When the thermal resistance between the chip and bottom plate rear face of the obtained package was measured, it was 0.2W/degree C.

[0032] By 0.7mm in example 3. thickness, a 405mmx340mm copper plate is used as a bottom plate 11, it oxide-film-removal-processes and silane coupling agent processing of this is carried out. Thermocompression bonding was carried out to the above-mentioned bottom plate 11 by having made into the frame material 12 the plasma surface treatment finishing polyimide film with one side adhesives of 150-micrometer thickness which opened 28 holes (vertical 4 train, width 7 train) of 15mm angle, and the substrate which has a crevice was formed. a crevice -- a high temperature conductivity pressure sensitive adhesive sheet -- {-- trade name: -- after sticking T-gon2000 and} made from the Sir magon INC, the semiconductor chip 2 of 14mm angle {staggered arrangement (2025 pin(s), diameter phiof putt (surface-preparation copper)100micrometer, and shortest pitch

370micrometer)} is stuck by pressure by face up.

[0033] Next, the dry-cleaning (film DF) {trade name of 68 micrometer thickness: ViaLux and} made from Dupont were laminated from the top with the vacuum laminator, patterning was performed using ultraviolet rays according to a part for the terminal area of a chip, and the phi75micrometer beer hall hole was formed. [photosensitive] Next, after performing a permanganic acid process (swelling, permanganic acid processing, and reduction) and performing surface roughening of DF, a conductor layer is formed on DF at the same time it performs electroless deposition and beer philharmonic electrolytic copper plating {the product made from a trade name:cube light and Ebara You G Light} and embeds a beer hole. At this time, conductor-layer thickness was 25 micrometers. Next, after carrying out half etching of the conductor layer and setting conductor-layer thickness to 10 micrometers, the etching dry film performed patterning of a conductor layer. The diameter of a land on beer set last shipment of phi100micrometer and wiring to 30 micrometers / 30 micrometers. CZ processing is performed to wiring on the obtained substrate, the Bahia hall beer-philharmonic-plated like the last process after a lamination in DF {trade name:ViaLux and the product made from Dupont} of 50-micrometer thickness and a conductor layer with a thickness of 10 micrometers are produced, and a circuit pattern is formed by etching. It accumulates one by one so that a conductor layer may turn into a total of nine layers at the same process as the following, and the solder resist which carried out opening of the terminal area to the maximum upper layer is formed. 28 semiconductor packages per substrate were obtained by finally cutting into the piece of an individual. When the thermal resistance between the chip and bottom plate rear face of the obtained package was measured, it was 0.1W/degree C.

[0034] The 405mmx340mm glass epoxy laminate {trade name which stuck copper foil of 18 micrometers of thickness on both sides by 1mm in example 4. thickness: Through-hole plating of 20-micrometer thickness is performed, and a thermal buyer hole is formed, and let this be a bottom plate 11, after DESUMIA [the part which mounts the semiconductor chip of epoxy multi and} by Matsushita Electric Works, Ltd. / four phi0.3mm through tubes / with a drill / open and] beforehand.

[0035] glass epoxy prepreg FR- of 250-micrometer thickness which opened 28 holes (vertical 4 train, width 7 train) of 15mm angle -- the press laminating was carried out to the above-mentioned bottom plate 11 by having made 4 {the Matsushita Electric Works, Ltd. make} into the frame material 12, and the substrate which has a crevice was formed. Under the present circumstances, it is in the condition that the thermal buyer hole is exposed to a crevice. the above-mentioned crevice -- a high temperature conductivity pressure sensitive adhesive sheet -- {-- trade name: -- after sticking T-gon2000 and} made from the Sir magon INC, the semiconductor chip 2 of 14mm angle {staggered arrangement (2025 pin(s), diameter phiof putt (surface-preparation copper)100micrometer, and shortest pitch 370micrometer)} is stuck by pressure by face up.

[0036] Next, photosensitive dry cleaning (film DF) {trade name:ViaLux of 68-micrometer thickness and} made from Dupont were laminated from the top with the vacuum laminator, patterning was performed using ultraviolet rays according to a part for the terminal area of a chip, and the phi75micrometer beer hall hole was formed. Next, after performing a permanganic acid process (swelling, permanganic acid processing, and reduction) and performing surface roughening of DF, a conductor layer is formed on DF at the same time it performs electroless deposition and beer philharmonic electrolytic copper plating {the product made from a trade name:cube light and Ebara You G Light} and embeds a beer hole. Under the present circumstances, it exposes to an inferior surface of tongue, and the inside of a thermal buyer is also galvanized. At this time, conductor-layer thickness was 25

micrometers. Next, after carrying out half etching of the conductor layer and setting conductor-layer thickness to 10 micrometers, the etching dry film performed patterning of a conductor layer. The diameter of a land on beer set last shipment of 100 micrometers and wiring to 30 micrometers / 30 micrometers. CZ processing is performed to wiring on the obtained substrate, the Bahia hall beer-philharmonic-plated like the last process after a lamination in DF {trade name:ViaLux and the product made from Dupont} of 50-micrometer thickness and a conductor layer with a thickness of 10 micrometers are produced, and a circuit pattern is formed by etching. It accumulates one by one so that a conductor layer may turn into a total of nine layers at the same process as the following, and the solder resist which carried out opening of the terminal area to the maximum upper layer is formed. 28 semiconductor packages per substrate were obtained by finally cutting into the piece of an individual. When the thermal resistance between the chip and bottom plate rear face of the obtained package was measured, it was 0.9W/degree C.

[0037] The semiconductor chip (2025 pin(s)) of 14mm angle and isomorphism-like crevice to mount were formed in 1.30mm angle of examples of a comparison, and 5mm thickness glass epoxy laminate {trade name:FR-4 and the Matsushita Electric Works make} by the mechanical cutting method, and the chip was pasted up on them by the silicone die bond agent by face up in the substrate crevice. From the top to furthermore, a photosensitive epoxy system interlayer-insulation-film {trade name: XP-9500cc and} made from SHIPUREI Far East were applied so that it might become 50 micrometers in thickness after hardening, and 90 degrees C dried for 45 minutes. According to a part for the terminal area of a chip, patterning was performed using ultraviolet rays, and phi75-micrometer beer hall hole was formed. Next, after performing the permanganic acid process (swelling, permanganic acid processing, and reduction) and performing surface roughening, when non-electrolytic copper plating and electrolytic copper plating were performed, plating was formed in the form where the beer hall configuration was met. Subsequently, copper patterning (last shipment=30micrometer / 30 micrometers) was performed by the photo etching method. Next, the multilayer interconnection was formed by the photograph beer build up method in the process same for wiring leading about. Since stat beer structure was not able to be taken at this time, a little beer of a vertical layer was shifted and the TEADO rope mold land was used. It could not let-two wiring pass but had to stop therefore, having to accumulate it a total of 17 layers among bumps. Although the package furthermore done tried DBA (direct bonding attaching) connection by the golden bump at the time of mother board connection, when it was pressurization, sedimentation of a terminal area took place, and good connection was not obtained. Moreover, when the thermal resistance between the chip and bottom plate rear face of the obtained package is measured, it is 1.8W/degree C, and with this configuration, the heat produced from the chip was not able to be missed efficiently.

[0038] The semiconductor chip (2025 pin(s)) of 14mm angle and isomorphism-like crevice to mount were formed in 2.30mm angle of examples of a comparison, and 1mm thickness copper plate by the mechanical cutting method, and the chip was pasted up on them by the silicone die bond agent by face up in the substrate crevice. From the top to furthermore, a photosensitive epoxy system interlayer-insulation-film {trade name:} made from XP-9500cc and SHIPUREI was applied so that it might become 50 micrometers in thickness after hardening, and 90 degrees C dried for 45 minutes. According to a part for the terminal area of a chip, patterning was performed using ultraviolet rays, and the phi75micrometer beer hall hole was formed. Next, after performing the permanganic acid process (swelling, permanganic acid processing, and reduction) and performing surface roughening, when non-electrolytic copper plating and electrolytic copper plating were

performed, plating was formed in the form where the beer hall configuration was met. Subsequently, copper patterning (last shipment=30micrometer / 30 micrometers) was performed by the photo etching method. Next, the multilayer interconnection was formed by the photograph beer build up method in the process same for wiring leading about. Since stat beer structure was not able to be taken at this time, a little beer of a vertical layer was shifted and the TEADO rope mold land was used. It could not let-two wiring pass but had to stop therefore, having to accumulate it a total of 17 layers among bumps. Although the semiconductor package further done although it was good when the thermal resistance between the chip and bottom plate rear face of the obtained package was measured tried DBA connection by the golden bump at the time of mother board connection, when it was pressurization, sedimentation of a terminal area took place, and good connection was not obtained. Moreover, when the solder reflow test of the obtained package was carried out, exfoliation occurred between the metal base section and an epoxy interlayer insulation film. Since this has many differential thermal expansions of a metal and an interlayer insulation film, and number of layerses of a build up layer, it originates in big stress having arisen.

[0039]

[Effect of the Invention] The substrate with which the 1st semiconductor device of this invention has a crevice, the semiconductor chip embedded in the above-mentioned crevice, The insulating layer which covers the above-mentioned semiconductor chip and a substrate front face, and has opening in the connection terminal area of the above-mentioned semiconductor chip, The above-mentioned opening is prepared in the layer flow section and the list which took the flow with the conductive ingredient at the above-mentioned insulating layer. the above-mentioned layer flow section and the flowing conductor -- with the resin composite material with which it is the semiconductor device equipped with wiring, and the above-mentioned substrate formed the thermal buyer, or the bottom plate which consists of a metal It has a larger through tube than the above-mentioned semiconductor chip, and it is the thing equipped with the frame material which consists of polyimide or resin composite material, excels [this bottom plate is pasted, and] in heat dissipation nature, and is effective in the ability to prevent the exfoliation at the time of a reflow.

[0040] the 2nd semiconductor device of this invention -- the 1st semiconductor device of the above -- setting -- a conductor -- the insulating layer which has on wiring stud beer which filled up the inside of beer with the conductive ingredient by the build up method, and a conductor -- it is what carried out the laminating of the wiring one by one, and is effective in high density wiring being possible.

[0041] In the 1st or 2nd semiconductor device of the above, resin composite material consists of resin, and glass fabrics, a nonwoven glass fabric, a polyamide system nonwoven fabric or a liquid crystal polymer system nonwoven fabric, the 3rd semiconductor device of this invention can prevent the exfoliation at the time of a reflow, and it is effective in excelling in thermal resistance.

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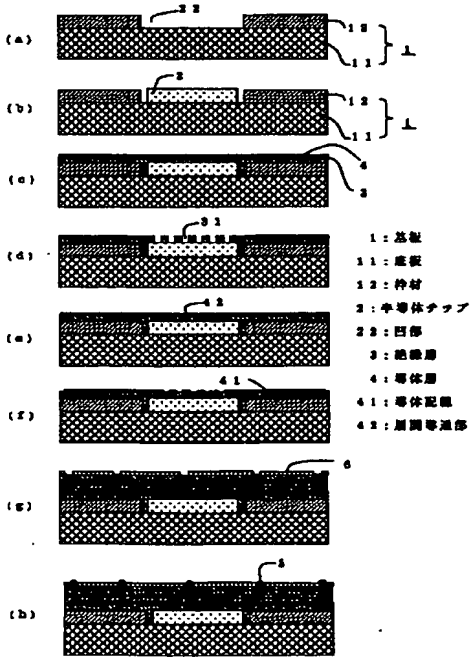
(71)出願人　000006013
三菱電機株式会社
東京都千代田区丸の内二丁目２番３号
(72)発明者　柳浦　聡
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内
(72)発明者　岡　誠次
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内
(72)発明者　藤岡　弘文
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内
(74)代理人　100102439
弁理士　宮田　金雄　（外１名）

(54)【発明の名称】　半導体装置

(57)【要約】
【課題】　高密度配線が可能で、リフロー時の剥離を防止された半導体装置を得る。
【解決手段】　基板１は金属からなる底板１１と樹脂複合材からなる枠材１２からなり、凹部２２を有する。凹部２２には半導体チップ２が埋め込まれ、その上には半導体チップ２の端子に層間導通部４２を有した絶縁層３が設けられ、絶縁層３には層間導通部と導通する導体配線４１を設けられ、さらに導体配線４１上にビルドアップ法により、スタッドビアを有する絶縁層と導体配線パターンが積層される。



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【特許請求の範囲】

【請求項１】　凹部を有する基板、上記凹部に埋め込まれた半導体チップ、上記半導体チップおよび基板表面を被覆し、上記半導体チップの接続端子部に開口を有する絶縁層、上記開口を導電性材料で導通を持たせた層間導通部、並びに上記絶縁層に設け、上記層間導通部と導通する導体配線を備えた半導体装置であって、上記基板が、サーマルバイヤーを形成した樹脂複合材料、または金属からなる底板と、この底板に接着され、上記半導体チップより大きい貫通孔を有し、ポリイミドまたは樹脂複合材料からなる枠材とを備えたものであることを特徴とする半導体装置。

【請求項２】　導体配線上にビルドアップ法により、ビア内を導電性の材料で充填したスタッドビアを有する絶縁層と導体配線を順次積層したことを特徴とする請求項１に記載の半導体装置。

【請求項３】　樹脂複合材料が樹脂と、ガラスクロス、ガラス不織布、ポリアミド系不織布または液晶ポリマー系不織布とで構成されていることを特徴とする請求項１または請求項２に記載の半導体装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、特に半導体チップ等の電子部品を実装した半導体装置に関するものである。

【０００２】

【従来の技術】従来、半導体インターポーザー基板を含んだパッケージのチップとインターポーザー基板の接続はワイヤーボンドかバンプ接続で行っているが、位置合わせ精度や電極の微細化に限界があり、０．４ｍｍ以下のピッチに対応するのは困難と考えられる。

【０００３】この対策として、高密度配線半導体チップをフェイスアップで基板に埋め込み、アウターバンプを引き出す方法が下記特許公報に記載されている。即ち、特開平４－２５０３８号公報には、基材凹部に、外部接続端子が表面に設けられたチップを埋め込み、この上に絶縁層を設けて上記外部接続端子部分にビアホールを形成した後、上層回路とバンプを形成し、それ以外の領域にソルダーレジストを形成したもので、上記基材としては、アルミニウム等の金属を用い、凹部をエッチングや機械的切削により設けたものや、熱硬化性樹脂等を用い、凹部を機械的切削や射出成形により設けたものが記載されている。

【０００４】また、特開平９－３２１４０８号公報には、上記公報と同様にして半導体チップを埋め込み、さらにビルドアップにより多層化したもので、半導体チップの外部接続端子として、スタッドバンプを用い、上記凹部は削り出しにより形成したものや、打ち抜かれたものが記載されている。

【０００５】また、特開平１－１７５２９７号公報には、一枚の基板の両面に、半導体チップの大きさの貫通孔を同一箇所に形成した二枚の基板を貼り合せた基板を用い、上記貫通孔に半導体チップを埋め込むことにより、高密度実装を行い、上記基板としてはガラスエポキシ等、銅張り積層板を用いたものが記載されている。

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【０００６】

【発明が解決しようとする課題】しかしながら、特開平４－２５０３８号公報に記載のものは、配線の展開が一層なので十分な引きまわしができず、放熱対策として金属基材表面に凹部を形成したものを用いているが、加工に高いコストがかかったり、リフロー時に、金属基材とこの上に設けた絶縁層との熱膨張の差により、金属基材と絶縁層の間に剥離が生じるという課題があった。また、樹脂からなる基材は、樹脂を機械加工したり、熱可塑性樹脂を射出成形して得ているが前者は高いコストがかかり、後者は離型剤を含有しているため上からコーティングする絶縁層との密着性が悪く、また、基材自体の熱膨張率が大きいため、半導体チップとの熱膨張係数差が大きく、リフロー時に半導体チップが割れたり、半導体チップとの間に剥離が生じやすいという課題があった。さらに後者ではチップの放熱性が悪く、チップの誤動作の原因となる。

【０００７】特開平９－３２１４０８号公報に記載のものは、スタッドバンプを用いるのでスタッドビア構造を得るのが困難であるため、高密度の配線引きまわしには不向きで、また、凹部を削り出した基板の材料は考慮されていないので、上記と同様、リフロー時に半導体チップ間に剥離が生じやすい、チップの放熱が不十分という課題があった。

【０００８】特開平１－１７５２９７号公報に記載のものは、第１、第２の基板（底板と枠材に相当）としてガラスエポキシ等銅張り積層板が用いられているが、熱伝導性が悪く放熱性に課題があった。

【０００９】本発明はかかる課題を解消するためになされたもので、放熱性に優れ、かつリフロー時の剥離の発生が防止された半導体装置か得られる。

【００１０】

【課題を解決するための手段】本発明に係る第１の半導体装置は、凹部を有する基板、上記凹部に埋め込まれた半導体チップ、上記半導体チップおよび基板表面を被覆し、上記半導体チップの接続端子部に開口を有する絶縁層、上記開口を導電性材料で導通をとった層間導通部、並びに上記絶縁層に設け、上記層間導通部と導通する導体配線を備えた半導体装置であって、上記基板が、サーマルバイヤーを形成した樹脂複合材料、または金属からなる底板と、この底板に接着され、上記半導体チップより大きい貫通孔を有し、ポリイミドまたは樹脂複合材料からなる枠材とを備えたものである。

【００１１】本発明に係る第２の半導体装置は、上記第１の半導体装置において、導体配線上にビルドアップ法

により、ビア内を導電性の材料で充填したスタッドビアを有する絶縁層と導体配線を順次積層したものである。

【００１２】本発明に係る第３の半導体装置は、上記第１または第２の半導体装置において、樹脂複合材料が樹脂と、ガラスクロス、ガラス不織布、ポリアミド系不織布または液晶ポリマー系不織布とで構成されているものである。

【００１３】

【発明の実施の形態】実施の形態１．図１（ａ）～（ｈ）は、本発明の実施の形態の半導体装置を製造する工程を示す説明図であり、図中、１は基板で、底板１１と枠材１２からなり、２は半導体チップ、２２は凹部、３は絶縁層、３１は開口、４は導体層、４１は導体配線、４２は層間導通部、５はバンプ、６はソルダーレジストである。

【００１４】本発明の実施の形態に係る凹部を有する基板１は、底板１１と枠材１２からなり枠材１２により基板１に凹部２２を形成し、枠材１２は半導体チップ２を底板１１にフェイスアップして載置できる半導体チップ２より大きい貫通孔を有したものである。

【００１５】底板１１としては、銅、４２アロイもしくはアルミ等の金属、またはサーマルバイヤーを形成した樹脂複合材料が用いられ、放熱性に優れるという効果がある。樹脂複合材料の樹脂成分としては、エポキシ、ポリパラフェニレン系樹脂またはＢＴレジンが用いられ、補強成分としては、液晶ポリマー不織布、ポリアミド繊維不織布、ガラスクロスまたはガラス不織布が用いられる。サーマルバイヤーとは底板上部（チップ実装側）に発生した熱を底板裏側に逃がすために形成されたスルーホールのことで、底板にφ０．２５ｍｍ～φ０．６ｍｍの貫通孔をドリル等であけ、その孔壁または孔全体に金属メッキまたは高熱伝導材料を充填したものである。高熱伝導材料とは有機樹脂に金属粒子やセラミック粒子を充填したもので熱伝導率が１．０Ｗ／ｍＫ以上のものである。底板にその裏面となる側に銅箔を貼り付けた樹脂複合材料を用い、サーマルバイヤーを設けた場合、サーマルバイヤーを伝わって裏側に回った熱はさらに底板裏側の銅箔に伝わりそこから空気中に効率的に放熱され、銅箔の上に放熱フィンやファンなどを設けることにより放熱性は一層強化される。また、底板にその両面に銅箔を貼り付けた樹脂複合材料を用いる場合は、半導体チップを設ける位置にサーマルバイヤーを形成して放熱性を維持し、かつ枠材を設ける位置の金属層を除くことにより枠材との密着性を向上することができる。また、底板１１として金属を用いると、放熱性に優れるとともに、半導体チップ２との熱膨張率差が小さいため、リフロー時の剥離を防止できる。

【００１６】また、枠材１２としては、上記樹脂複合材料プリプレグの他、ポリイミドフィルムまたは液晶ポリマーフィルムが用いられるが、ポリイミドフィルムは耐熱性に優れるとともに、熱膨張率が小さく、絶縁層との密着性が良いためリフロー時の剥離を防止できる。

【００１７】さらに、本発明に係る半導体パッケージは底板の片側に絶縁層と導体配線を積んでゆくので、後工程において反りが発生しないようなある程度剛性の高い底板、枠板が好ましく、例えば底板に銅を用いる場合は０．５ｍｍ厚以上の銅板が好ましく、枠板の厚さは用いる半導体チップの厚さと同程度が良い。

【００１８】また、ビルドアップ法により絶縁層と導体配線を積層して多層配線を施す場合、本実施の形態に係わる上記基板を用いることにより、チップから発生する熱を効率よく外部に放熱することができ、チップの温度上昇を押さえチップの誤動作や破壊を防止するという効果が得られる。

【００１９】次に、図１を用いて、本発明の実施の形態の半導体装置を製造する工程を説明する。まず、上記枠材１２と底板１１を貼り合わせることにより凹部２２を有する基板１を得る｛図１（ａ）｝。貼り合わせは熱プレスまたは熱ラミネーターが量産性の点で好ましい。枠材が複合材プリプレグの場合はそのまま貼り合わせ可能であるが、樹脂フィルムの場合接着剤を用いる必要がある。

【００２０】次に、上記のようにして得られた基板１の凹部２２に半導体チップをフェイスアップして貼り付ける｛図１（ｂ）｝。貼り付けには高放熱性の観点から熱伝導性の高いダイボンド剤を用いることが好ましい。熱伝導性の高いダイボンド材とはエポキシ樹脂やポリイミド樹脂中に銅、銀、アルミナ、ダイヤモンド、窒化珪素または窒化硼素などのフィラーを高充填したもので、熱伝導率としては、２．０Ｗ／ｍ・Ｋ以上が好ましい。

【００２１】次に上から一層目の絶縁層３を形成する（図１（ｃ））。絶縁層３は液状樹脂、フィルム樹脂、ＲＣＣ（Ｒｅｓｉｎ　Ｃｏａｔｅｄ　Ｃｏｐｐｅｒ）のいずれでも良いが、多層に積層する観点から上層の平坦性は重要であり、その点を考慮するとフィルムまたはＲＣＣが好ましく、図は絶縁層としてＲＣＣを用いた場合を示し、絶縁層に導体層４が貼られている。絶縁層がＲＣＣの場合、積層は熱プレスまたは真空ラミネーターを用い、フィルムの場合は真空ラミネーターを用いる。

【００２２】絶縁層３に開口３１（バイアホール）を形成する｛図１（ｄ）｝が、絶縁層が感光性を有している場合は露光、現像により一括でバイアホールを形成することが可能であり、感光性を有していない場合はレーザー光を用いてバイアホールを形成する。レーザー光としては炭酸ガスレーザー、エキシマレーザー、ＹＡＧレーザーの高調波が好ましい。エキシマレーザーはマスクを用いたエリア一括露光が可能であり、他のレーザーは一穴ずつのビーム照射となる。また、レーザーでバイアホールを形成した場合、バイアホール底部に絶縁膜残渣が残ったり、また絶縁膜に銅箔が付いていない場合、絶縁

膜に銅メッキ密着性を付与させるために、絶縁膜のパターニング工程の後、過マンガン酸処理工程、プラズマ処理工程またはオゾン水処理工程の何れかを施す必要がある。

【００２３】得られたバイアホール３１に導電性材料を充填して層間導通部４２を形成する｛図１（ｅ）｝。層間導通部４２は開口３１に導電性材料を充填することにより形成するので、スタッドビア形成が可能になり、高密度実装が可能となる。充填する方法として銅メッキを用いる方法と導電性ペーストを用いる方法がある。絶縁層にＲＣＣを用いた場合、導電性ペーストでバイアホールを充填することによりメッキレスでの配線形成が可能となる。導電性ペーストでバイアホールを充填する場合は減圧下で印刷可能であるスクリーン印刷を用いるのが好ましい、但し設備の都合上減圧下で印刷出来ない場合でも、加圧下で硬化することによりボイドレスの充填が可能である。絶縁層に銅箔が付いていない場合は、メッキによりバイアホールを充填する方法が工程を短縮できる点で好ましい。バイアホール充填を銅メッキで行う場合は通常の無電解メッキ後、特殊なビアフィル銅メッキメッキ用電解メッキ液を用いる必要があるがこれらは市販されており、容易に入手可能である。但しビアフィル銅メッキでビアを充填した場合、絶縁膜表面にも厚いＣｕメッキが形成される場合もあるので、その場合は必要に応じ表面銅メッキ膜厚をハーフエッチングまたは研磨によって薄くする必要がある。

【００２４】次に得られた導体層４を通常のサブトラスト法により導体配線４１を形成する｛図１（ｆ）｝。また微細な配線形成を行う場合はセミアデティブ銅メッキ法を適用しても良い。この方法は無電解メッキ形成後、メッキレジストパターンを形成し、開口部に電解メッキを積み上げ、配線形成を行った後、レジストを剥離し、パターン間に残った無電解メッキをソフトエッチングで除去することにより微細で厚い銅配線パターンを得るためのものである。

【００２５】さらに絶縁層形成、バイアホール形成、バイアホール導体接続（又は充填）、配線形成を繰り返すことによりビルドアップ配線層の多層化が達成され、本発明の実施の形態の半導体装置を得ることができ、さらに、最外層パターン上にソルダーレジスト６を形成し｛図１（ｇ）｝、接続用のバンプ５やボールを形成する（図１（ｈ）｝。

【００２６】

【実施例】実施例１．厚さ０．５ｍｍの４０５ｍｍ×３４０ｍｍ銅板を底板１１とし、酸化膜除去処理後、シランカップリング剤処理する。次に、２５０μｍ厚ＦＲ－５｛商品名：エポキシマルチＲ－１７６６，松下電工（株）製｝ガラスクロス・エポキシプリプレグに１５ｍｍ角の孔を２８個（縦４列、横７列）あけたものを枠材１２とし、これを上記銅板に、プレス積層することにより、凹部２２を設けた基板１を得る。

【００２７】上記凹部２２に、高熱伝導性粘着シート｛商品名：Ｔ－ｇｏｎ２０００，サーマゴンＩＮＣ製｝を貼り付けた後、１４ｍｍ角の半導体チップ２｛ｐｉｎ数２０２５、バット（表面処理された銅）径φ１００μｍ、最短ピッチ３７０μｍの千鳥配列｝を、フェイスアップで圧着する。次に、６８μｍ厚の感光性ドライフィルム（ＤＦと略す）｛商品名：ＶｉａＬｕｘ，Ｄｕｐｏｎｔ（株）製｝を真空ラミネーターで上からラミネートし、チップの端子部分に合わせて紫外線を用いてパターニングを行い、φ７５μｍビアホール穴を形成する。次に、過マンガン酸工程（膨潤・過マンガン酸処理・還元）を行い、ＤＦの表面粗化を行った後、無電解メッキおよびビアフィル電解銅メッキ｛商品名：キュープライト，荏原ユージーライト（株）製｝を施しビア穴を埋め込むと同時にＤＦ上に導体層を形成する。このとき導体層厚は２５μｍであった。次に導体層をハーフエッチングし、導体層厚を１０μｍとしたのちエッチングドライフィルムにより導体層のパターニングを行った。ビア上のランド径はφ１００μｍ、配線Ｌ／Ｓは３０μｍ／３０μｍとした。

【００２８】得られた基板上の配線を表面処理（ＣＺ処理）｛商品名：エッチボンド，メック（株）製｝し、５０μｍ厚の感光性ドライフィルム｛商品名：ＶｉａＬｕｘ，Ｄｕｐｏｎｔ（株）製｝をラミネート後、前工程と同様、ビアフィルメッキされたバイアホールおよび厚さ１０μｍの導体層を作製し、配線パターンをエッチングにより形成する。以下同様な工程で導体層が合計９層になるように順次積み上げ、最上層に端子部を開口させたソルダーレジストを形成する。最後に個片にカットすることにより、基板１枚につき２８個の半導体パッケージを得た。得られたパッケージのチップ・底板裏面間の熱抵抗を測定したところ０．１℃／Ｗであった。

【００２９】実施例２．厚さ０．５ｍｍの４０５ｍｍ×３４０ｍｍの４２アロイ板を底板１１とし、これをシランカップリング剤処理した。その後、１５ｍｍ角の孔を２８個（縦４列、横７列）あけた２５０μｍ厚液晶ポリマー不織布・エポキシプリプレグを枠材１２とし、これを上記アロイ板にプレス積層し、凹部２２を設けた基板１を得た。凹部２２に高熱伝導性粘着シート｛商品名：Ｔ－ｇｏｎ２０００，サーマゴンＩＮＣ製｝を貼り付けた後、１４ｍｍ角の半導体チップ２｛ｐｉｎ数２０２５、バット（表面処理済みの銅）径φ１００μｍ、最短ピッチ３７０μｍの千鳥配列｝を、フェイスアップで圧着する。

【００３０】次に、ＲＣＣ（樹脂厚１００μｍ、銅箔厚１２μｍ）｛商品名：Ｒ－０８７０，松下電工（株）製｝を熱プレスで上から積層し、チップの端子部分に合わせて炭酸ガスレーザーを用いてパターニングを行い、φ７５μｍビアホール穴を形成した。但しこのあとビア

底に残った樹脂残渣を除去するため酸素プラズマでホールクリーニングを行った。次にエポキシ樹脂に銀コート銅フィラーを含有した導電性ペースト｛商品名：京都エレックス社（株）製｝を真空スクリーン印刷機を用いてビア穴に埋め込み、熱硬化した後はみ出した部分を研磨により除去した。

【００３１】次にエッチングドライフィルムにより導体層のパターニングを行った。ビア上のランド径はφ１００μｍ、配線のＬ／Ｓは３０μｍ／３０μｍとした。得られた基板上の配線に黒化処理を施し、５０μｍ厚のＲＣＣを積層後、前工程と同様レーザー穴あけ、導電性ペーストが充填されたバイアホールおよび配線パターンをエッチングにより形成する。以下同様な工程で導体層が合計９層になるように順次積み上げ、最上層に端子部を開口させたソルダーレジストを形成する。最後に個片にカットすることにより、基板１枚につき２８個の半導体パッケージを得た。得られたパッケージのチップ・底板裏面間の熱抵抗を測定したところ０．２Ｗ／℃であった。

【００３２】実施例３．厚さ０．７ｍｍで４０５ｍｍ×３４０ｍｍの銅板を底板１１とし、これを酸化膜除去処理、シランカップリング剤処理する。１５ｍｍ角の孔を２８個（縦４列、横７列）あけた１５０μｍ厚の片面接着剤付きプラズマ表面処理済みポリイミドフィルムを枠材１２として、上記底板１１に熱圧着し、凹部を有する基板を形成した。凹部に高熱伝導性粘着シート｛商品名：Ｔ－ｇｏｎ２０００，サーマゴンＩＮＣ製｝を貼り付けた後、１４ｍｍ角の半導体チップ２｛ｐｉｎ数２０２５、バット（表面処理銅）径φ１００μｍ、最短ピッチ３７０μｍの千鳥配列｝を、フェイスアップで圧着する。

【００３３】次に６８μｍ厚の感光性ドライフィルム（ＤＦ）｛商品名：ＶｉａＬｕｘ，Ｄｕｐｏｎｔ（株）製｝を真空ラミネーターで上からラミネートし、チップの端子部分に合わせて紫外線を用いてパターニングを行い、φ７５μｍのビアホール穴を形成した。次に過マンガン酸工程（膨潤・過マンガン酸処理・還元）を行い、ＤＦの表面粗化を行った後、無電解メッキおよびビアフィル電解銅メッキ｛商品名：キューブライト，荏原ユージーライト（株）製｝を施しビア穴を埋め込むと同時にＤＦ上に導体層を形成する。このとき導体層厚は２５μｍであった。次に導体層をハーフエッチングし、導体層厚を１０μｍとしたのちエッチングドライフィルムにより導体層のパターニングを行った。ビア上のランド径はφ１００μｍ、配線のＬ／Ｓは３０μｍ／３０μｍとした。得られた基板上の配線にＣＺ処理を施し、５０μｍ厚のＤＦ｛商品名：ＶｉａＬｕｘ，Ｄｕｐｏｎｔ（株）製｝をラミネート後、前工程と同様、ビアフィルメッキされたバイアホールおよび厚さ１０μｍの導体層を作製し、配線パターンをエッチングにより形成する。以下同様な工程で導体層が合計９層になるように順次積み上げ、最上層に端子部を開口させたソルダーレジストを形成する。最後に個片にカットすることにより、基板１枚につき２８個の半導体パッケージを得た。得られたパッケージのチップ・底板裏面間の熱抵抗を測定したところ０．１Ｗ／℃であった。

【００３４】実施例４．厚さ１ｍｍで両面に厚１８μｍの銅箔を貼り付けた４０５ｍｍ×３４０ｍｍのガラスエポキシ積層板｛商品名：エポキシマルチ、松下電工（株）製｝の、半導体チップを実装する部分に予め４個のφ０．３ｍｍの貫通孔をドリルであけ、デスミアした後、２０μｍ厚のスルーホールめっきを行い、サーマルバイヤーホールを形成しこれを底板１１とする。

【００３５】１５ｍｍ角の孔を２８個（縦４列、横７列）あけた２５０μｍ厚のガラスエポキシプリプレグＦＲ－４｛松下電工（株）製｝を枠材１２として、上記底板１１にプレス積層し、凹部を有する基板を形成した。この際、凹部にはサーマルバイヤーホールが露出している状態にある。上記凹部に高熱伝導性粘着シート｛商品名：Ｔ－ｇｏｎ２０００，サーマゴンＩＮＣ製｝を貼り付けた後、１４ｍｍ角の半導体チップ２｛ｐｉｎ数２０２５、バット（表面処理銅）径φ１００μｍ、最短ピッチ３７０μｍの千鳥配列｝を、フェイスアップで圧着する。

【００３６】次に、６８μｍ厚の感光性ドライフィルム（ＤＦ）｛商品名：ＶｉａＬｕｘ，Ｄｕｐｏｎｔ（株）製｝を真空ラミネーターで上からラミネートし、チップの端子部分に合わせて紫外線を用いてパターニングを行い、φ７５μｍのビアホール穴を形成した。次に過マンガン酸工程（膨潤・過マンガン酸処理・還元）を行い、ＤＦの表面粗化を行った後、無電解メッキおよびビアフィル電解銅メッキ｛商品名：キューブライト，荏原ユージーライト（株）製｝を施しビア穴を埋め込むと同時にＤＦ上に導体層を形成する。この際、下面に露出してサーマルバイヤー内もめっきされる。このとき導体層厚は２５μｍであった。次に導体層をハーフエッチングし、導体層厚を１０μｍとしたのちエッチングドライフィルムにより導体層のパターニングを行った。ビア上のランド径は１００μｍ、配線のＬ／Ｓは３０μｍ／３０μｍとした。得られた基板上の配線にＣＺ処理を施し、５０μｍ厚のＤＦ｛商品名：ＶｉａＬｕｘ，Ｄｕｐｏｎｔ（株）製｝をラミネート後、前工程と同様、ビアフィルメッキされたバイアホールおよび厚さ１０μｍの導体層を作製し、配線パターンをエッチングにより形成する。以下同様な工程で導体層が合計９層になるように順次積み上げ、最上層に端子部を開口させたソルダーレジストを形成する。最後に個片にカットすることにより、基板１枚につき２８個の半導体パッケージを得た。得られたパッケージのチップ・底板裏面間の熱抵抗を測定したところ０．９Ｗ／℃であった。

【００３７】比較例１．３０ｍｍ角、５ｍｍ厚ガラスエポキシ積層板｛商品名：ＦＲ－４，松下電工製｝に、実装する１４ｍｍ角の半導体チップ（ｐｉｎ数２０２５）と同形状の凹部を機械的切削法により形成し、チップをフェイスアップでシリコーンダイボンド剤にて基板凹部に接着した。さらにその上から感光性エポキシ系層間絶縁膜｛商品名：ＸＰ－９５００ｃｃ，シプレィ・ファーイースト（株）製｝を硬化後の厚さ５０μｍになるように塗布し、９０℃４５分乾燥した。チップの端子部分に合わせて紫外線を用いてパターニングを行い、φ７５μｍビアホール穴を形成した。次に過マンガン酸工程（膨潤・過マンガン酸処理・還元）を行い、表面粗化を行った後、無電解銅メッキ・電解銅メッキを行ったところビアホール形状に沿った形でメッキが形成された。ついでフォトエッチング法にて銅のパターニング（Ｌ／Ｓ＝３０μｍ／３０μｍ）を行った。次に配線引きまわしのため同様なプロセスでフォトビアビルドアップ法にて多層配線を形成した。このときスタットビア構造がとれないため上下層のビアを少しずらしてテアドロップ型ランドを用いた。そのためバンプ間に配線を２本通すことができず、合計１７層積み上げなければならなくなった。さらにできあがったパッケージはマザーボード接続の際金バンプでＤＢＡ（ダイレクト　ボンディング　アタッチ）接続を試みたが加圧の際に端子部の沈降が起こり、良好な接続が得られなかった。また、得られたパッケージのチップ・底板裏面間の熱抵抗を測定したところ１．８Ｗ／℃であり、この構成ではチップから生じた熱を効率良く逃がすことができなかった。

【００３８】比較例２．３０ｍｍ角、１ｍｍ厚銅板に、実装する１４ｍｍ角の半導体チップ（ｐｉｎ数２０２５）と同形状の凹部を機械的切削法により形成し、チップをフェイスアップでシリコーンダイボンド剤にて基板凹部に接着した。さらにその上から感光性エポキシ系層間絶縁膜｛商品名：ＸＰ－９５００ｃｃ，シプレィ（株）製｝を硬化後の厚さ５０μｍになるように塗布し、９０℃４５分乾燥した。チップの端子部分に合わせて紫外線を用いてパターニングを行い、φ７５μｍのビアホール穴を形成した。次に過マンガン酸工程（膨潤・過マンガン酸処理・還元）を行い、表面粗化を行った後、無電解銅メッキ・電解銅メッキを行ったところビアホール形状に沿った形でメッキが形成された。ついでフォトエッチング法にて銅のパターニング（Ｌ／Ｓ＝３０μｍ／３０μｍ）を行った。次に配線引きまわしのため同様なプロセスでフォトビアビルドアップ法にて多層配線を形成した。このときスタットビア構造がとれないため上下層のビアを少しずらしてテアドロップ型ランドを用いた。そのためバンプ間に配線を２本通すことができず、合計１７層積み上げなければならなくなった。得られたパッケージのチップ・底板裏面間の熱抵抗を測定したところ、良好であったが、さらにできあがった半導体パッケージはマザーボード接続の際金バンプでＤＢＡ接続を試みたが加圧の際に端子部の沈降が起こり、良好な接続が得られなかった。また得られたパッケージを半田リフローテストしたところ金属基材部とエポキシ層間絶縁膜の間に剥離が発生した。これは金属と層間絶縁膜の熱膨張差およびビルドアップ層の層数が多いために大きな応力が生じたことに起因する。

【００３９】

【発明の効果】本発明の第１の半導体装置は、凹部を有する基板、上記凹部に埋め込まれた半導体チップ、上記半導体チップおよび基板表面を被覆し、上記半導体チップの接続端子部に開口を有する絶縁層、上記開口を導電性材料で導通をとった層間導通部、並びに上記絶縁層に設け、上記層間導通部と導通する導体配線を備えた半導体装置であって、上記基板が、サーマルバイヤーを形成した樹脂複合材料、または金属からなる底板と、この底板に接着され、上記半導体チップより大きい貫通孔を有し、ポリイミドまたは樹脂複合材料からなる枠材とを備えたもので、放熱性に優れ、リフロー時の剥離が防止できるという効果がある。

【００４０】本発明の第２の半導体装置は、上記第１の半導体装置において、導体配線上にビルドアップ法により、ビア内を導電性の材料で充填したスタッドビアを有する絶縁層と導体配線を順次積層したもので、高密度配線が可能であるという効果がある。

【００４１】本発明の第３の半導体装置は、上記第１または第２の半導体装置において、樹脂複合材料が樹脂と、ガラスクロス、ガラス不織布、ポリアミド系不織布または液晶ポリマー系不織布とで構成されているもので、リフロー時の剥離が防止でき、耐熱性に優れるという効果がある。

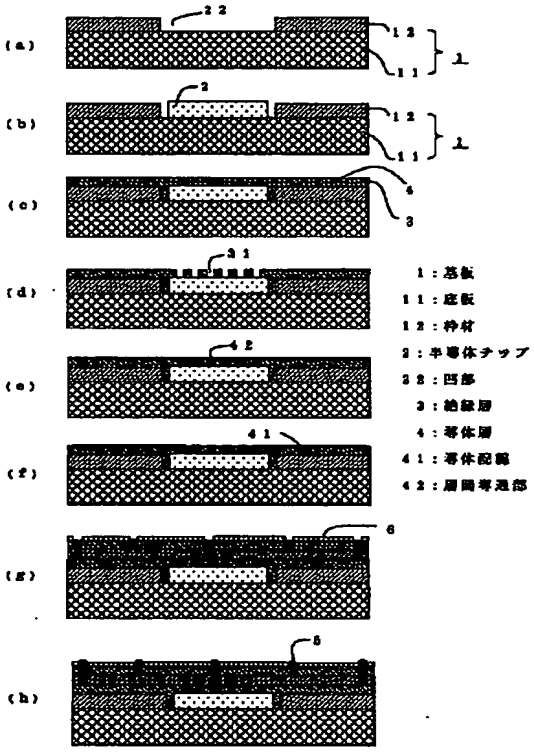
【図面の簡単な説明】

【図１】　本発明の実施の形態の半導体装置を製造する工程を示す説明図である。

【符号の説明】

１　基板、１１　底板、１２　枠材、２　半導体チップ、２２　凹部、３　絶縁層、４　導体層、４１　導体配線、４２　層間導通部。

【図１】


(a)
(b)
(c)
(d)
(e)
(f)
(g)
(h)
22
12
11
1
2
4
3
31
42
41
6
5
1：基板
11：底板
12：枠材
2：半導体チップ
22：凹部
3：絶縁層
4：導体層
41：導体配線
42：層間導通部